Atty. Docket No. MP0299

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

Pantas SUTARDJA et al. : GROUP ART UNIT: 2611

APPLICATION NO: 10/634,218 :

FILED: AUGUST 4, 2003 : EXAMINER: WANG, Ted M.

FOR: ARCHITECTURES, CIRCUITS, SYSTEMS AND METHODS FOR REDUCING LATENCY IN DATA COMMUNICATIONS

I hereby certify that this document is being facsimile transmitted to the USPTO or deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on MARCH 3, 2008.

By: Jennie Heaton
Jennie Heaton

DECLARATION UNDER 37 C.F.R. 1.131

Mail Stop AMENDMENT
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

Now comes Chee Hoe CHU, who declares and states that:

1. I am currently employed by Marvell Semiconductor, Inc. ("Marvell"). I am a Manager in the Advanced Interface Technology Group at Marvell. I have been continuously employed by Marvell since 2002. Prior to joining Marvell, I worked as a design engineer for Infineon Technologies North America and for NEC Electronics Singapore Pte. Ltd.

2. I received a Bachelor's degree (Honors) in Electrical & Electronic Engineering from Nanyang Technological University (Singapore).

3. I understand that at least one independent claim of the above-identified application is directed to an architecture for transferring data from a first device to a second device, comprising:

a) a clock recovery loop receiving said data from said first device, said clock recovery loop providing a recovered clock signal;

b) a filter circuit configured to filter information from said recovered clock signal and provide a transmitter clock adjustment signal that adjusts said transmitter clock in response to inputs from (i) said clock recovery loop and (ii) a transmitter clock circuit; and

c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal.

4. I further understand that at least a second independent claim of the above-identified application is directed to a multiport device, comprising:

a) a plurality of receivers, each coupled to a unique one of a plurality of clock recovery loops,

b) a plurality of transmitters, each coupled to a unique one of a plurality of filter circuits receiving recovered clock information from a corresponding one of the plurality of clock recovery loops, and

c) a plurality of data paths for transferring data from one of the plurality of receivers to one of the plurality of transmitters.

5. The architecture defined in paragraph 4 and the multiport device defined in paragraph 5 above were diligently manufactured and tested during the time period including April 23, 2003 to May 28, 2003.

6. Attached hereto as Exhibit A is a redacted copy of the System Validation Report page for a first version of a multiport integrated circuit device designed and sold by Marvell (and manufactured according to Marvell's instructions). Pages 5-9 and 11 of Exhibit A contain data showing that the first version of the multiport integrated circuit device analyzed in Exhibit A has multiplexer ("mux")-to-multiplexer latency that is unacceptably large for a number of intended uses of the integrated circuit device.

7. The date of the System Validation Report in Exhibit A is before April 23, 2003.

8. Attached hereto as Exhibit B is a redacted copy of the System Validation Report page for version 2.0 of the same multiport integrated circuit device designed and sold by Marvell (and manufactured according to Marvell's instructions) analyzed in Exhibit A. On information and belief, I understand that the multiport integrated circuit device designed and sold by Marvell is an embodiment of the multiport device defined in paragraph 5 above and contains a circuit embodying the architecture defined in paragraph 4 above (the "working embodiment").

9. The date of the System Validation Report in Exhibit B for version 2.0 of the multiport integrated circuit device is May 28, 2003.

10. On information and belief, the integrated circuit analyzed in Exhibit B was taped out at a wafer manufacturing fab prior to April 24, 2003.

11. On information and belief, wafers containing the integrated circuit analyzed in Exhibit B and described in paragraph 8 above were manufactured after tape out. On information and belief, at least part of the manufacturing process occurred after April 24, 2003.

12. The manufactured integrated circuit described in paragraph 11 was diligently tested after manufacturing.

13. One of the results of testing the manufactured integrated circuit was that round-trip multiplexer latency was reduced to 4 data words (see Exhibit B, page 5, the first 4 rows in the "Mux Latency" table, under the column labeled "Remarks"). On information and belief, this

result is evidence that the working embodiment had been successfully reduced to practice on or before May 28, 2003.

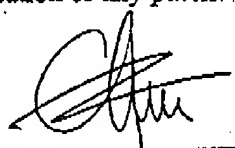
14. Attached hereto as Exhibit C is a redacted copy of the Characterization Report page for version 2.0 of the multiport integrated circuit device analyzed in Exhibit B.

15. The date of the Characterization Report in Exhibit B for version 2.0 of the multiport integrated circuit device is May 28, 2003.

16. The data and results in Exhibit C from testing the manufactured integrated circuit show that round-trip multiplexer latency between the host (either of the far left-hand blocks in Figure 5, Section 7.3 of Exhibit C) and the device (far right-hand block in Figure 5, Section 7.3 of Exhibit C) was reduced to 4 data words (see Exhibit B, page 5, the first 4 rows in the "Mux Latency" table, under the column labeled "Remarks"). On information and belief, the results shown in Figures 31-47 of Exhibit C are evidence that the working embodiment had been successfully reduced to practice on or before May 13, 2003.

17. Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.



Chee Hoe CHU

1/11/2008
Date

EXHIBIT A

Marvell	[redacted]	
	Document number: Alpha test report Release date: [redacted]	Revision number: [redacted] Page 1 of 14

[redacted]

System Validation Report

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1. PURPOSE

This document is intended to provide the progress status of the [redacted] post silicon testing [redacted]

[redacted]

Mux Latency			
Reading Host : [redacted] (FIFO = 31) Device : [redacted] (Rev FIFO = 31)	• [redacted] • Host and device [redacted] dongles CFG[1:0]=10B. • Host [redacted]'s recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 192ns. • Latency (HOLD till HOLDA) with [redacted] is 508ns. • Latency introduced [redacted] is 316ns.	2/Y	Latency introduced [redacted] is 13 Dword
Writing Host : [redacted] (FIFO = 31) Device : [redacted] (Rev FIFO = 31)	• [redacted] • Host and device [redacted] dongles CFG[1:0]=10B. • Dev [redacted]'s recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 190ns. • Latency (HOLD till HOLDA) with [redacted] is 528ns. • Latency introduced [redacted] is 338ns.	2/Y	Latency introduced [redacted] is 12 Dword

Reading Host : [redacted] (FIFO = 31) Device : [redacted] (Rev FIFO = 31)	• [redacted] • Host [redacted] 's recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 160ns. • Latency (HOLD till HOLDA) with [redacted] is 510ns. • Latency introduced [redacted] is 360ns.	2/Y	Latency introduced [redacted] is 13 Dword
Writing Host : [redacted] (FIFO = 31) Device : [redacted] (Rev FIFO = 31)	• [redacted] • UAI/UAO pins [redacted] lifted for register configuration. • Dev [redacted] 's recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 190ns. • Latency (HOLD till HOLDA) with [redacted] is 500ns. • Latency introduced [redacted] is 310ns.	2/Y	Latency introduced [redacted] is 12 Dword

Reading Host : [redacted] (FIFO = 31) Device : [redacted] (Rev FIFO = 31)	• [redacted] • Device [redacted] dongles CFG[1:0]=10B. • Host [redacted]'s recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 180ns. • Latency (HOLD till HOLDA) with [redacted] is 520ns. • Latency introduced [redacted] is 340ns.	2/Y	Latency introduced [redacted] is 13 Dword
Writing Host : [redacted] (FIFO = 31) Device : [redacted] (Rev FIFO = 31)	• [redacted] • Device [redacted] dongles CFG[1:0]=10B. • Dev [redacted]'s recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 190ns. • Latency (HOLD till HOLDA) with [redacted] is 500ns. • Latency introduced [redacted] is 310ns.	2/Y	Latency introduced [redacted] is 12 Dword

Marvell	[redacted]	
MARVELL	Document number: Alpha test report Release date: [redacted]	Revision number: [redacted] Page 8 of 14

Reading Host [redacted] (FIFO = 31) Device : [redacted] HDD	• [redacted] • Host [redacted] 's recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) without [redacted] is 250ns. • Latency (HOLD till HOLDA) with [redacted] is 590ns. • Latency introduced [redacted] is 340ns.	2/Y	Latency introduced [redacted] is 13 Dword
Writing Host : [redacted] (FIFO = 31) Device : [redacted] HDD	• [redacted] • Host [redacted] 's recv FIFO watermark set to 31. • Latency (HOLD till HOLDA) . without [redacted] is 170ns. • With [redacted], transfer error due to too much latency.	2/Y	X

Reading Host : [redacted] (FIFO = 48) Device : [redacted] (Rev FIFO = 48)	• [redacted] • Host and device [redacted] dongles CFG[1:0]=10B. • No change to host [redacted]'s recv FIFO watermark is needed as default is 48. • Latency (HOLD till HOLDA) without [redacted] is 184ns. • Latency (HOLD till HOLDA) with [redacted] is 516ns. • Latency introduced [redacted] is 332ns.	2/Y	Latency introduced [redacted] is 13 Dword
Writing Host : [redacted] (FIFO = 48) Device : [redacted] (Rev FIFO = 48)	• [redacted] • Host and device [redacted] dongles CFG[1:0]=10B. • No change to host [redacted]'s recv FIFO watermark is needed as default is 48. • Latency (HOLD till HOLDA) without [redacted] is 180ns. • Latency (HOLD till HOLDA) with [redacted] is 520ns. • Latency introduced [redacted] is 340ns.	2/Y	Latency introduced [redacted] is 13 Dword

4. UP TODATE BUGS FOUND BY THE SV GROUP

1) Latency is too big. [redacted]

EXHIBIT B

Marvell	[redacted] R2.0	
MARVELL	Document number: Alpha test report Release date: [redacted]	Report Revision number: [redacted] Page 1 of 11

[redacted]

System Validation Report

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1. PURPOSE

This document is intended to provide the progress status of the [redacted] post silicon testing. [redacted]

[redacted]

Marvell	[redacted] R2.0	
MARVELL	Document number: Alpha test report Release date: [redacted]	Report Revision number: [redacted] Page 5 of 11

[redacted]

Mux Latency

Description	Who	Detail	test date	results	comment	Remarks
The latency from RX to TX is less than 30ns.	[redacted]	portA - portC	13-May	1/Y		4 dwords (4 x 26 ns)
		port B -port C	13-May	1/Y		4 dwords (4 x 26 ns)
		portC - port A	13-May	1/Y		4 dwords (4 x 26 ns)
		portC - port B	13-May	1/Y		4 dwords (4 x 26 ns)

[redacted]

EXHIBIT C

MARVELL

[redacted] R2.0 [redacted] Characterization Report

[redacted]

7.3. OOB Tolerance Test ([redacted] Setup)

Because [redacted] is [redacted] a [redacted] multiplexor, it needs to connect with [redacted] on the host port and [redacted] on the device port to establish the [redacted] communication during OOB test. Due to the latency between host [redacted] and device [redacted], the idle time between COMRESET and COMWAKE generated by pattern generator should be [redacted]
The Test setup of Host0 port is shown in Figure below.

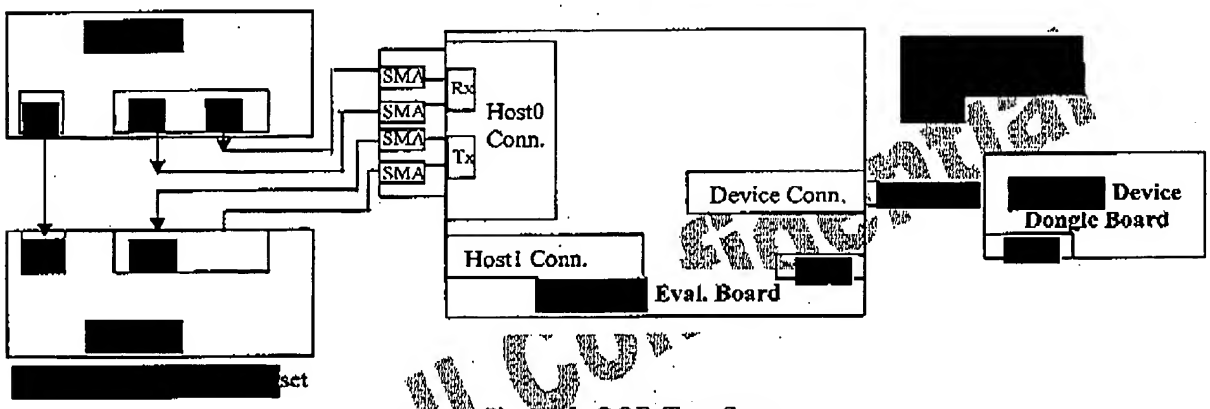

Figure 5: OOB Test Setup

To force continuous detection of COMWAKE [redacted] even though COMRESET/COMINIT is not being detected, [redacted] internal register bit R33 [8] [redacted] set to 1 when COMRESET/COMINIT is off threshold (loaded file are CRST04 and CRST05). Table below summarizes the OOB tolerance test results. [redacted] passed all combination of the COMRESET/COMINIT and COMMWAKE spacing settings.

DC control COMRESET/COMINIT spacing	COMWAKE spacing	File	Host	Device	Fig
[redacted] (normal)	[redacted] (normal)	CRST01	Passed	Passed	Figure 31, 40
[redacted] (min)	[redacted] (normal)	CRST02	Passed	Passed	Figure 32, 41
[redacted] (max)	[redacted] (normal)	CRST03	Passed	Passed	Figure 33, 42
[redacted] (off threshold)	[redacted] (normal)	CRST04	Passed	Passed	Figure 34, 43
[redacted] (off threshold)	[redacted] (normal)	CRST05	Passed	Passed	Figure 35
[redacted] (normal)	[redacted] (min)	CWAKE02	Passed	Passed	Figure 36, 44
[redacted] (normal)	[redacted] (max)	CWAKE03	Passed	Passed	Figure 37, 45
[redacted] (normal)	[redacted] (off threshold)	CWAKE04	Passed	Passed	Figure 38, 46
[redacted] (normal)	[redacted] (off threshold)	CWAKE 05	Passed	Passed	Figure 39, 47

Table 4: OOB Tolerance Test [redacted] Setup)

[redacted]

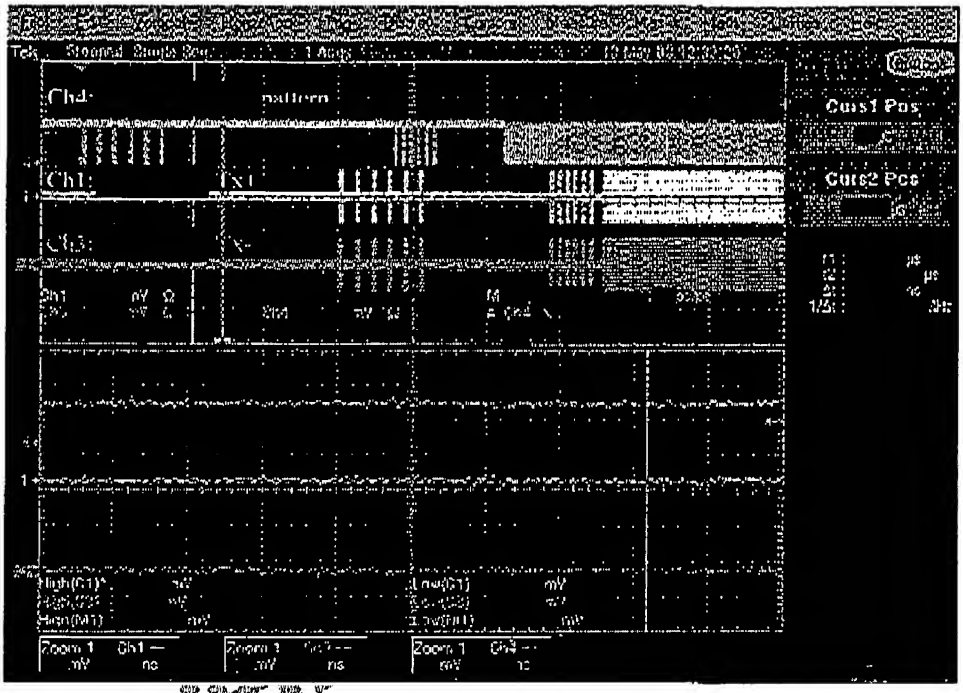

Figure 31: Host0 OOB CRST1 Test

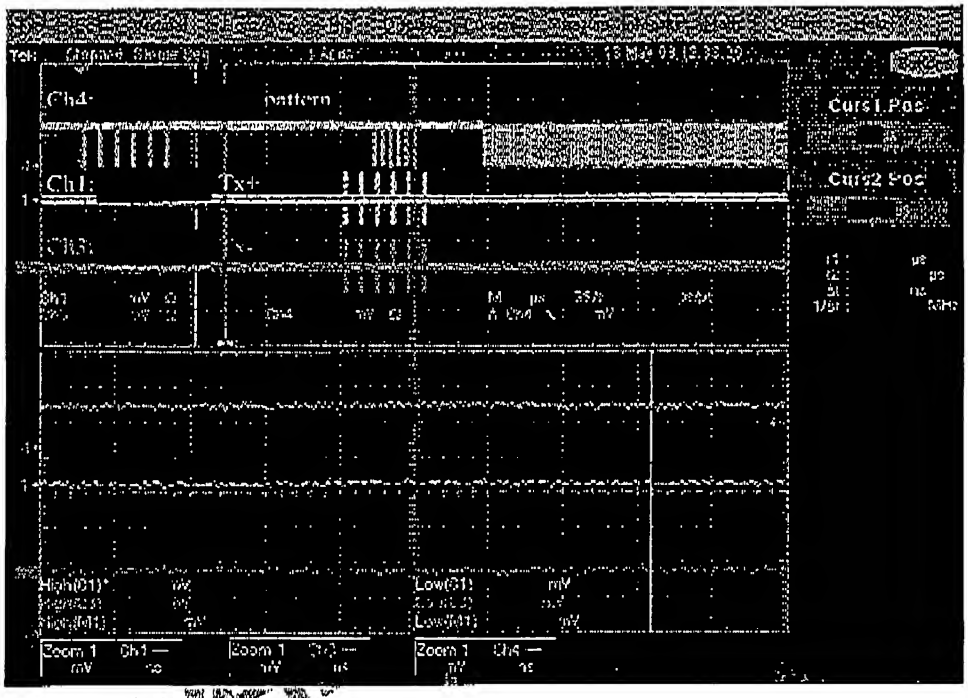

Figure 32: Host0 OOB CRST2 Test

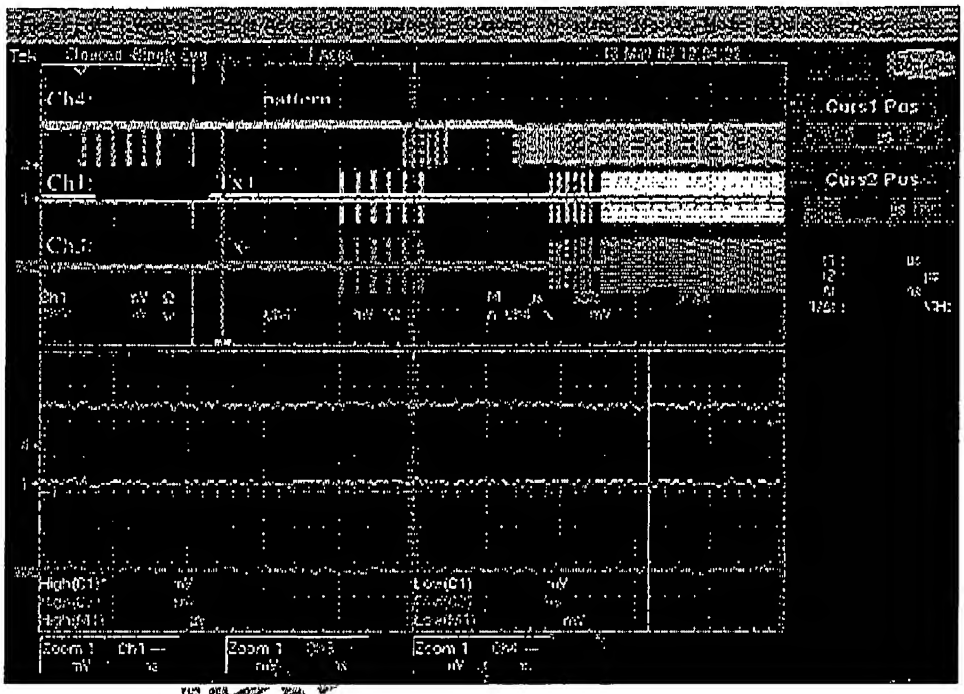

Figure 33: Host0 OOB CRST3 Test

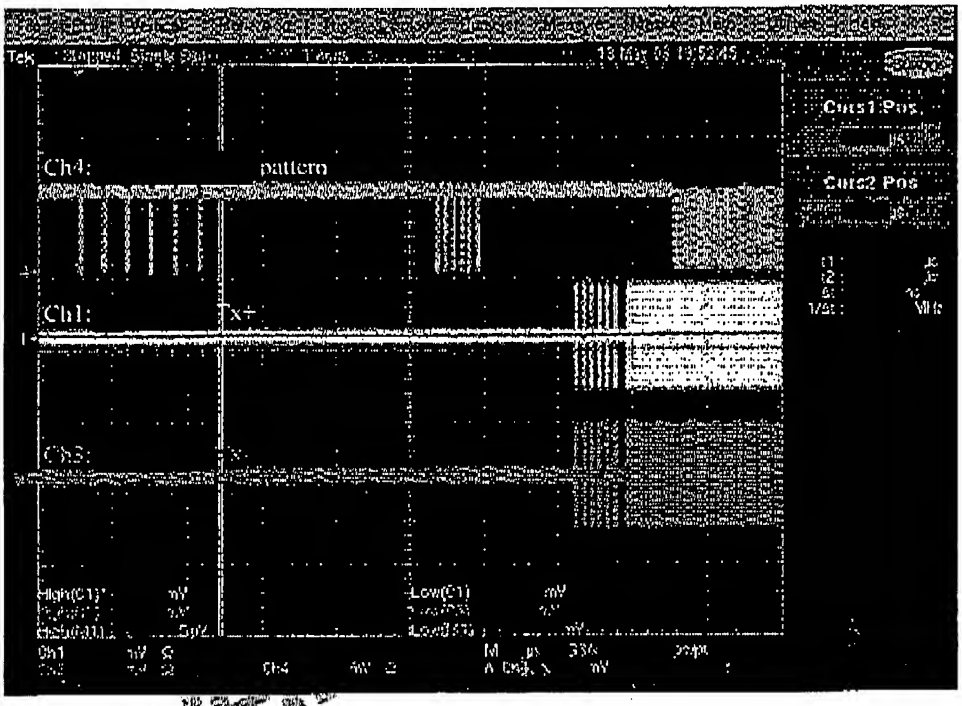

Figure 34: Host0 OOB CRST4 Test

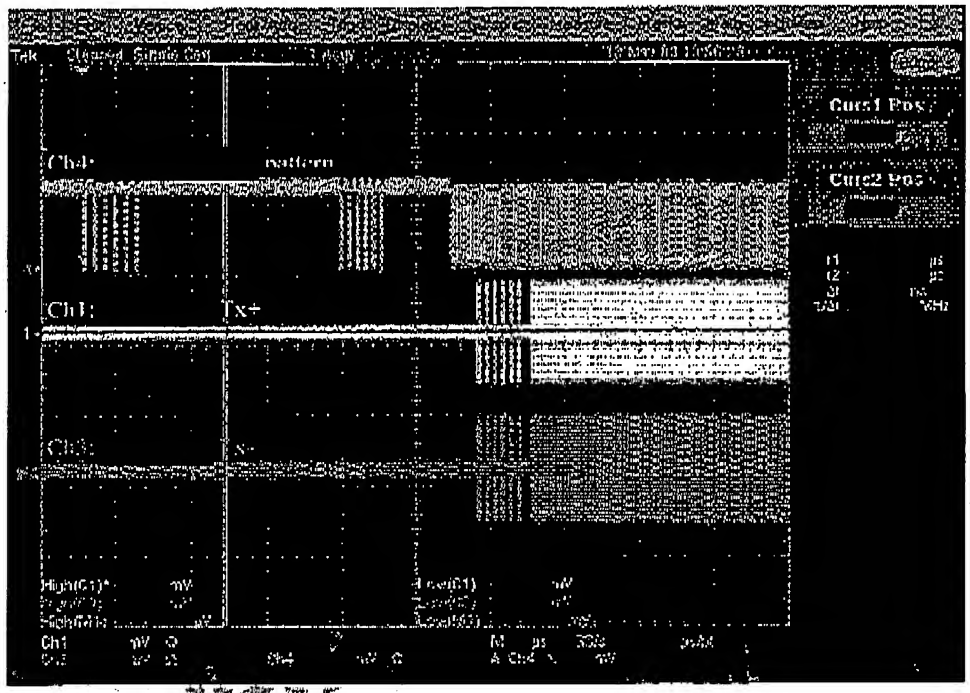

Figure 35: Host0 OOB CRST5 Test

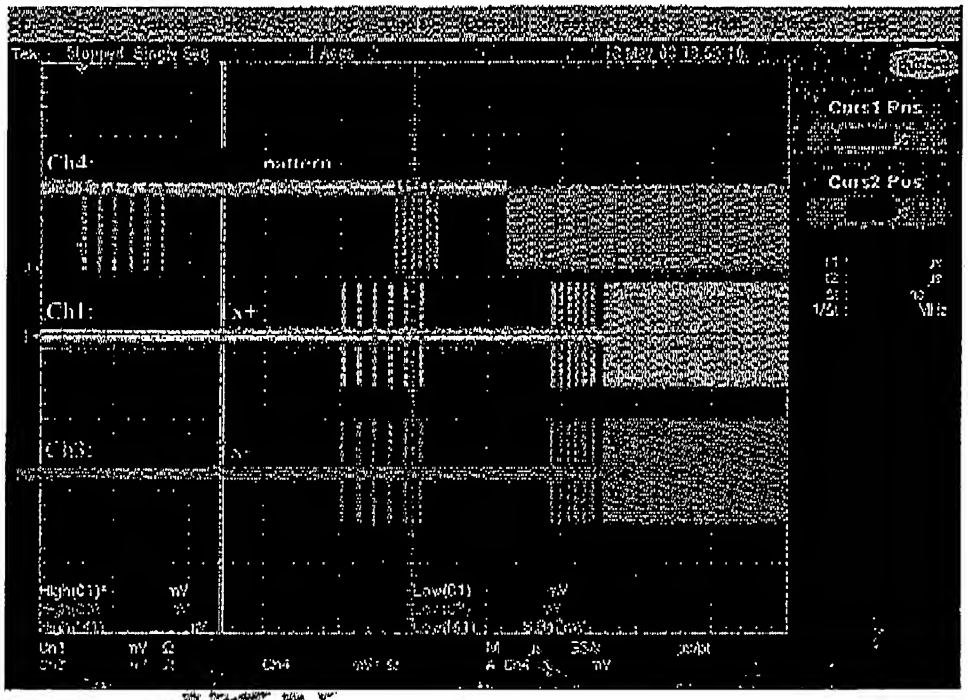

Figure 36: Host0 OOB CWAKE2 Test

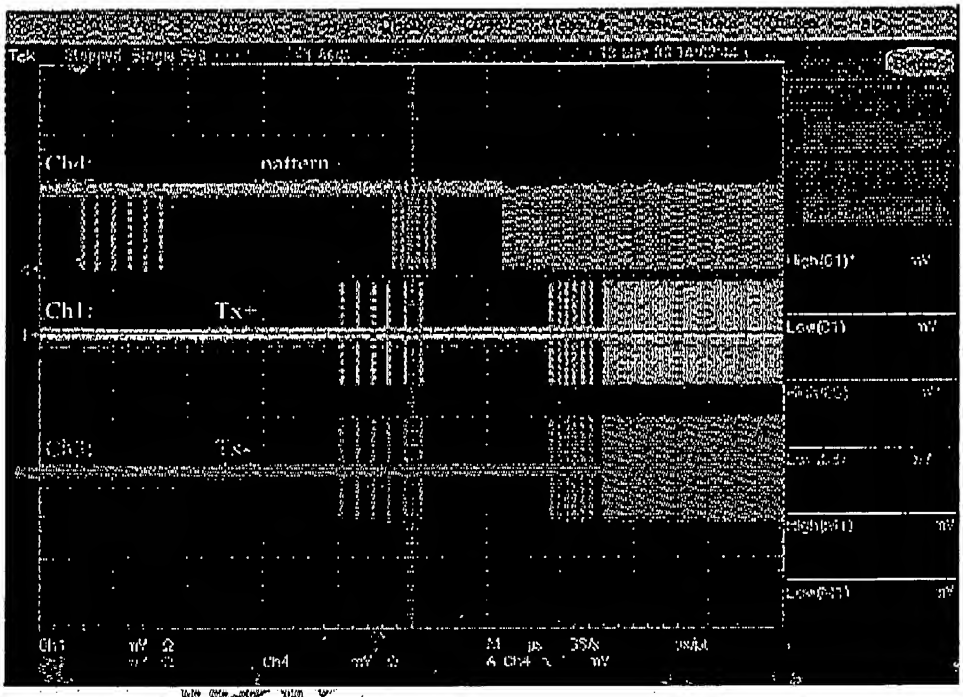

Figure 37: Host0 OOB CWAKE3 Test

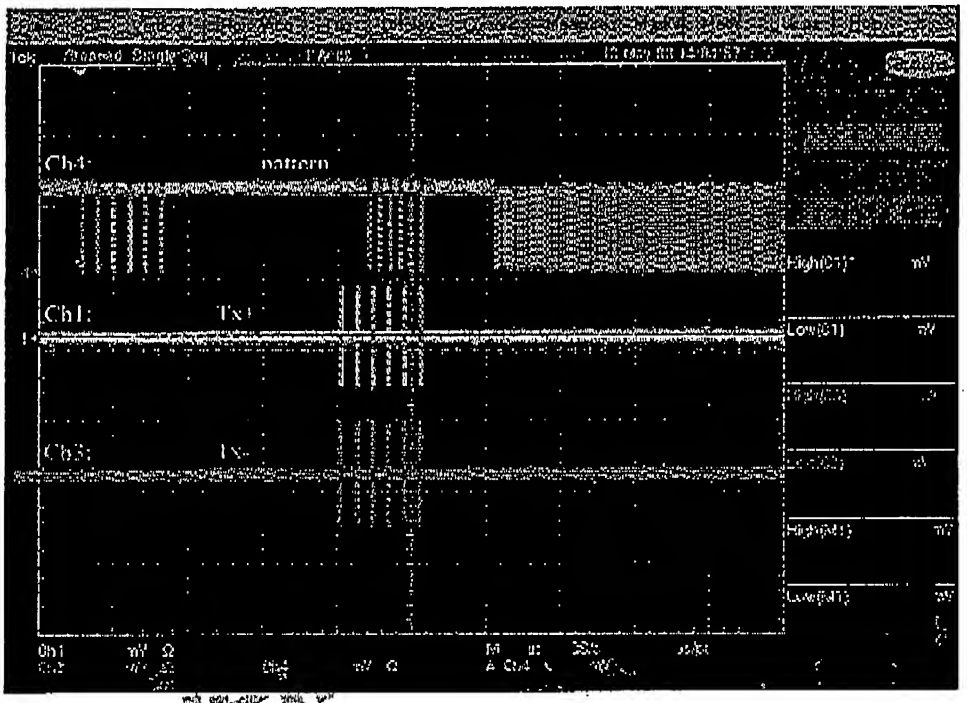

Figure 38: Host0 OOB CWAKE4 Test

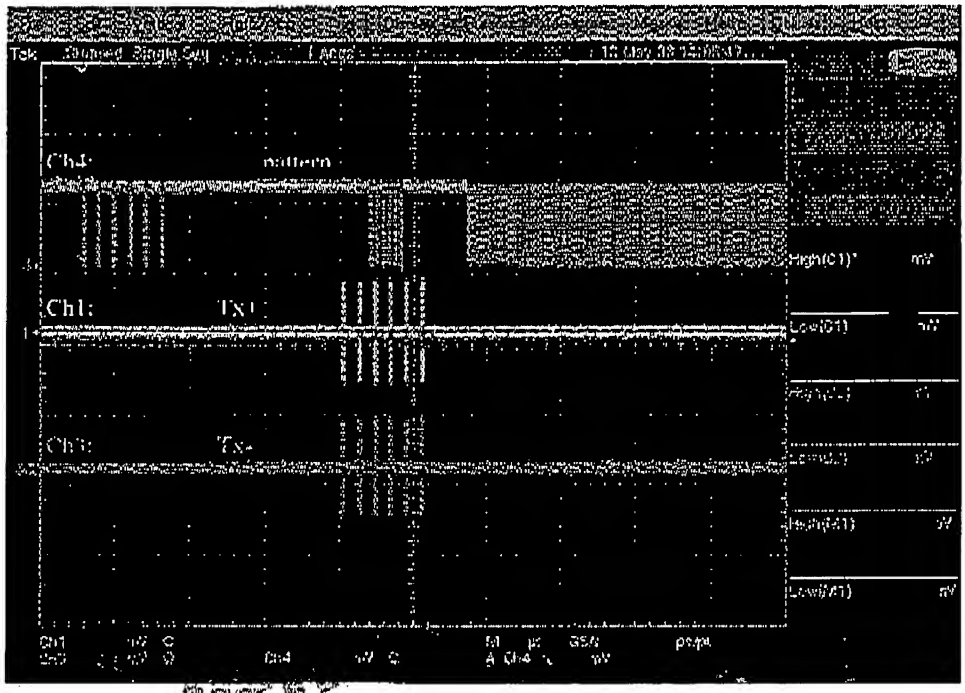

Figure 39: Host0 OOB CWAKE5 Test

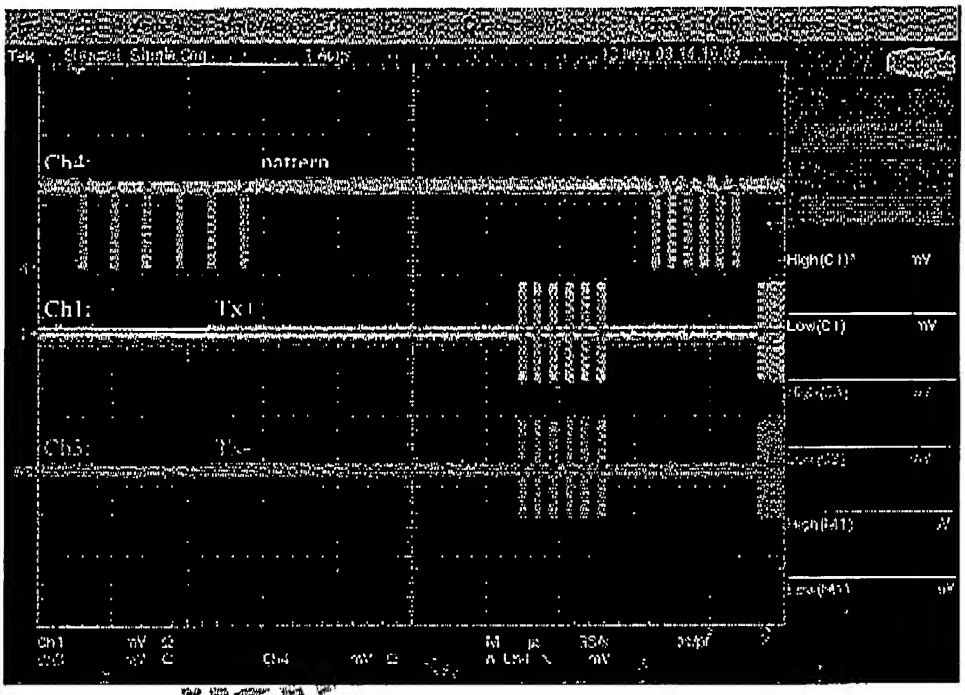

Figure 40: Device OOB CRST1 Test

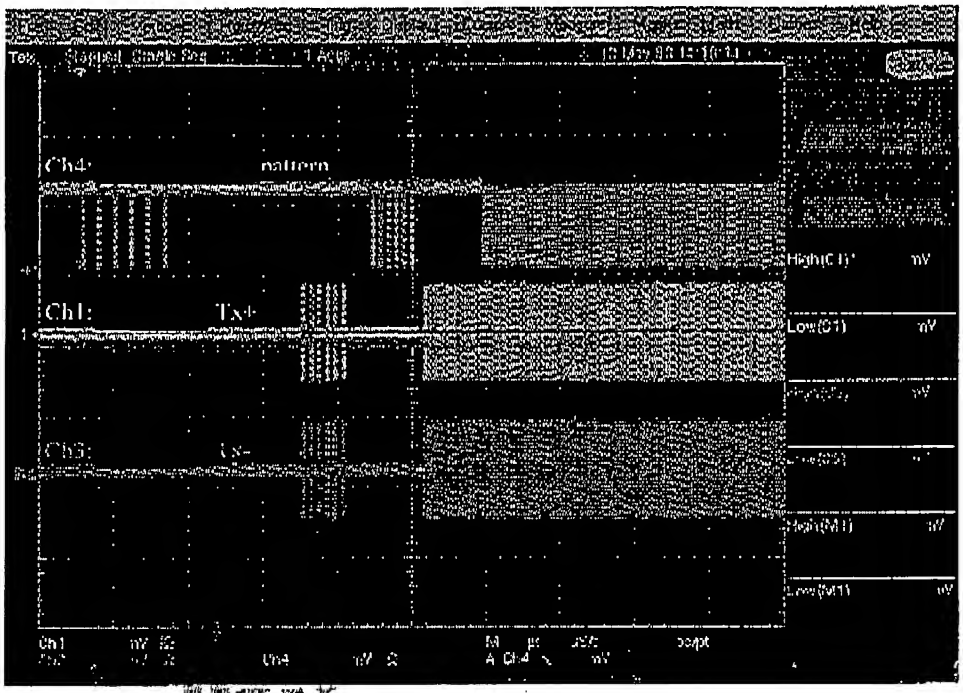

Figure 41: Device OOB CRST2 Test

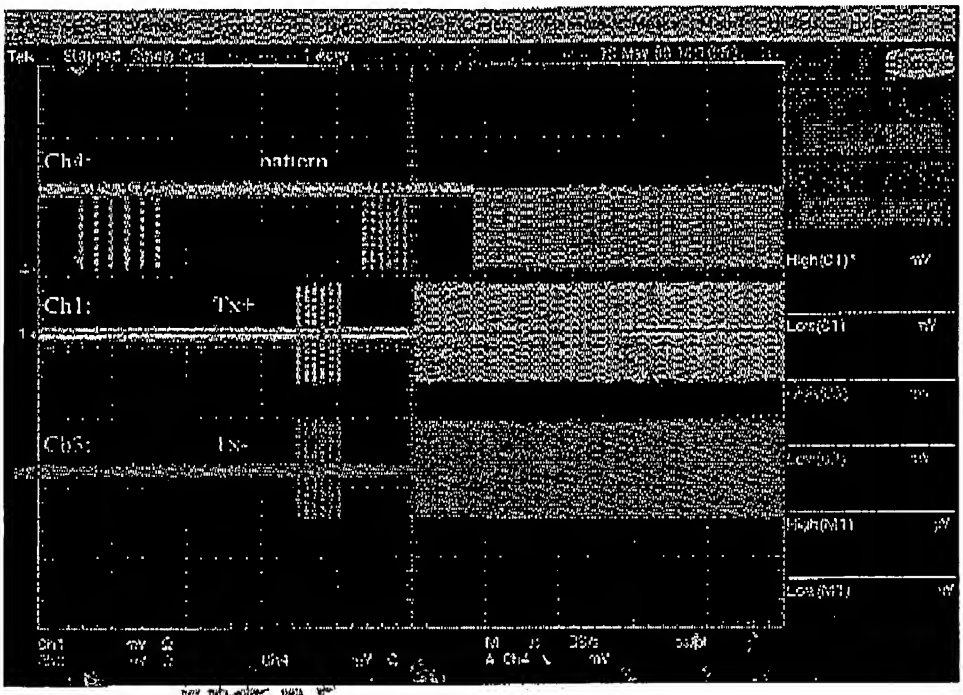

Figure 42: Device OOB CRST3 Test

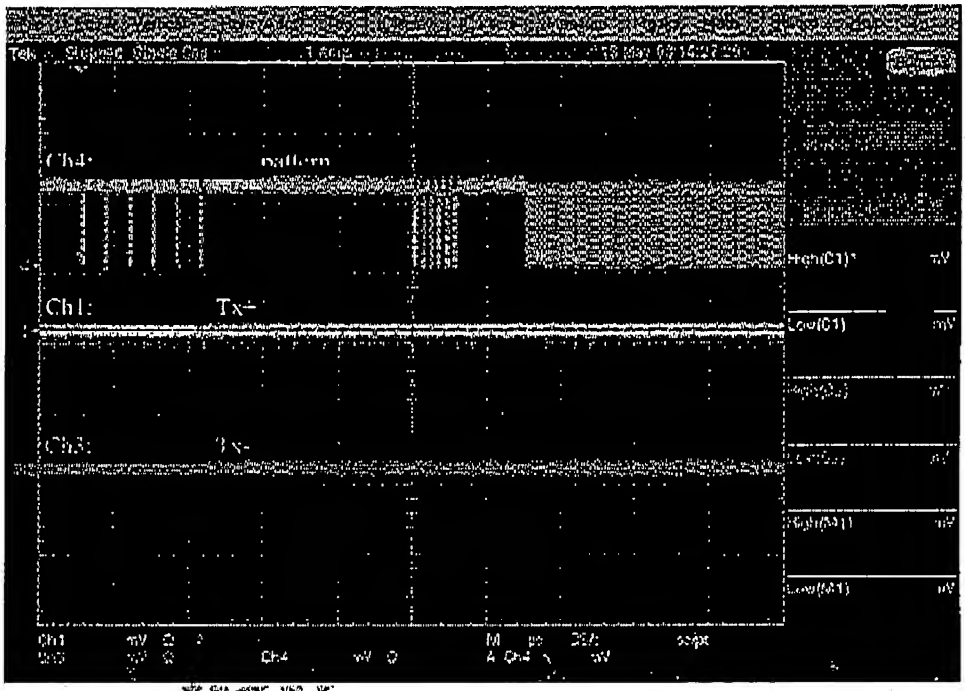

Figure 43: Device OOB CRST4 Test

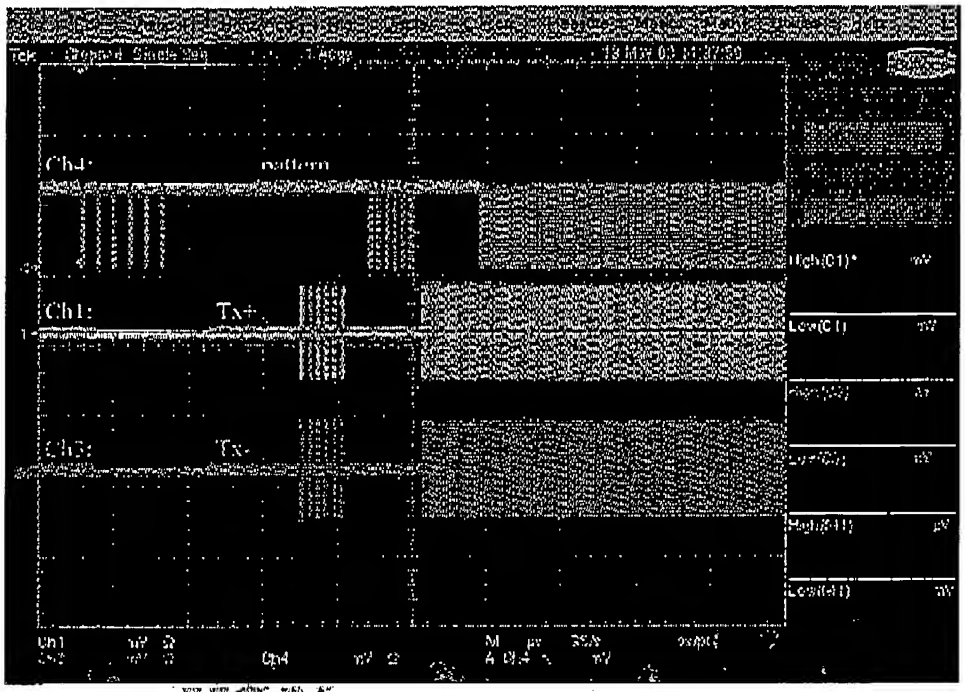

Figure 44: Device OOB CWAKE2 Test

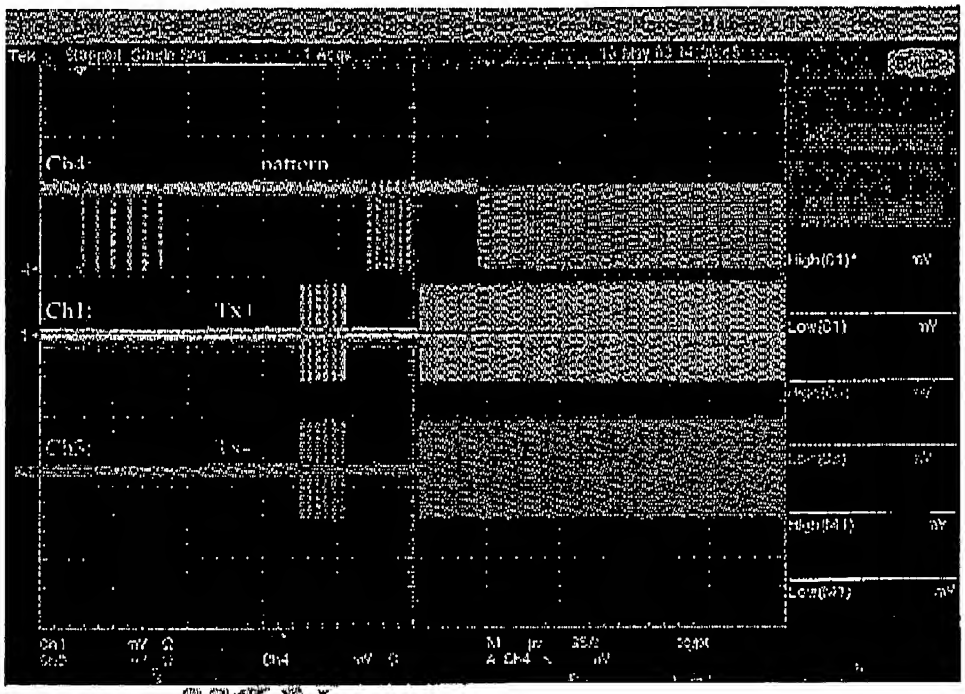

Figure 45: Device OOB CWAKE3 Test

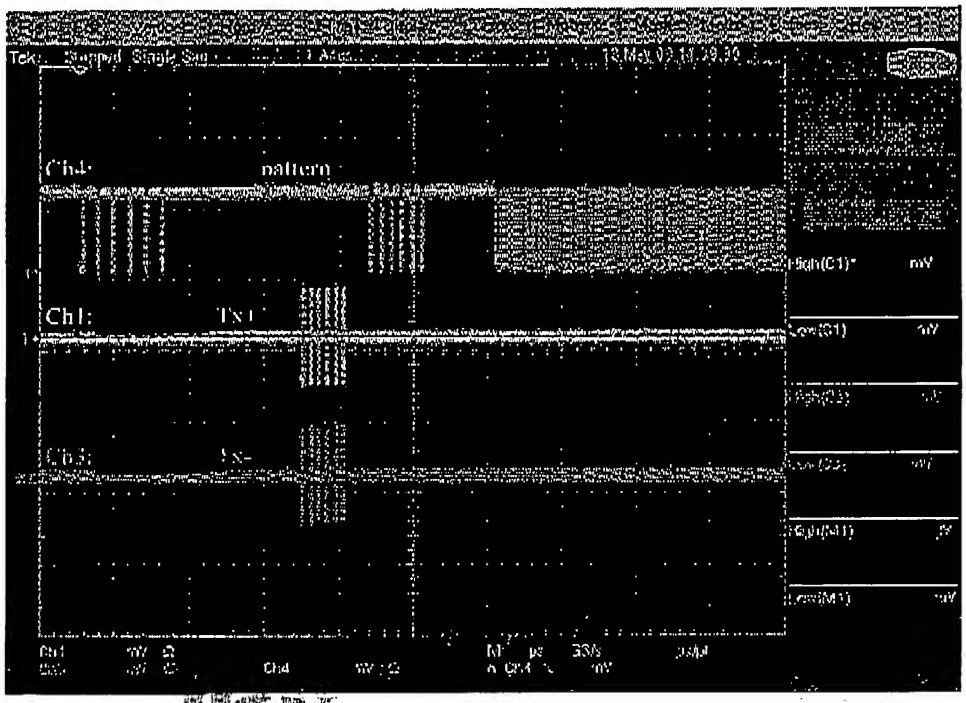

Figure 46: Device OOB CWAKE4 Test

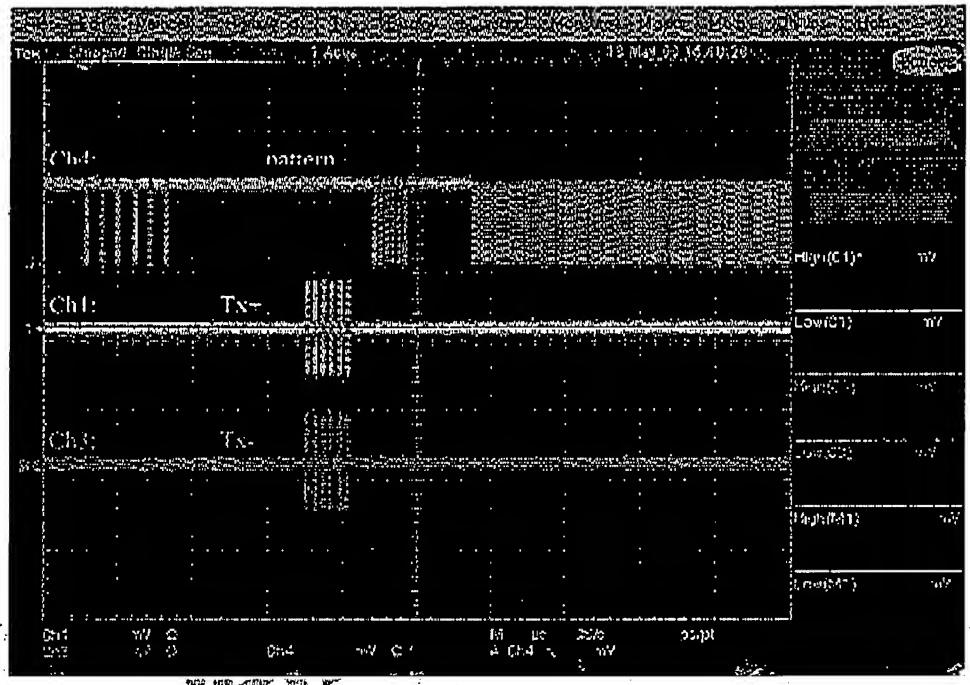

Figure 47: Device OOB CWAKE5 Test